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Title	:	**System for Emulating Graphics Operations**			
Inventors	:	**John Harper**			
Serial No.	:	**10/826,744**	Filed	:	**April 16, 2004**
Examiner	:	**Maurice L. Mcdowell Jr.**	Art Unit	:	**2628**
Docket	:	**P3356US1 (119-0036US)**	Customer	:	**61947**

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APPEAL BRIEF

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I. Real Party in Interest

Apple Inc. is the real party in interest.

II. Related Appeals and Interferences

None.

III. Status of Claims

Claims 1-75 are cancelled. Claims 76-80 stand rejected. Claims 76-80 are appealed.

IV. Status of Amendments

None.

V. Summary of Claimed Subject Matter

This section provides a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, referring to the specification by paragraph number and to the drawings by reference characters as required by 37 C.F.R. § 41.37(c)(l)(v). Paragraph numbers refer to the application as filed on 16 April 2004. Citation to the specification and/or drawings does not imply that limitations from the specification and drawings should be read into the corresponding claim element. Additionally,

references are not necessarily exhaustive, and various claim elements may also be described at other locations within the specification and/or drawings.

Generally, Appellant claims a method (independent claim 76) and a computer-readable medium (independent claim 80) for emulating a second microprocessor with a first microprocessor to increase the ability to simultaneously process multiple frames of an image with two effects. More specifically:

Independent claim 76 recites a method of applying two effects to an image, the method comprising the steps of

- using a first microprocessor to apply a first effect to a first frame of said image, said first microprocessor applying said first effect while emulating a second microprocessor (¶ 32, Figs 2a-b and ¶¶ 125-128, Figs 15a-c);
- using said second microprocessor to apply a second effect to said first-effected frame, applying said first effect to a next frame by said first microprocessor approximately during the time that said second microprocessor is applying said second effect to said first-effected frame (¶ 32, Figs 2a-b and ¶¶ 125-128, Figs 15a-c).

Independent claim 80 recites a computer-readable medium having computer executable instructions for performing the method recited in claim 76 (¶ 32, Figs 2a-b and ¶¶ 125-128, Figs 15a-c).

VI. Grounds of rejection to be reviewed on appeal

Claims 76-80 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U.S. Patent No. 6,115,054 to Giles ("Giles") in view of U.S. Patent Publication No. 2003/0009748 to Glanville et al. ("Glanville").

VII. Argument

The claims stand or fall together. Appellant presents arguments for independent claim 76 applicable to each of the noted rejections. Independent claim 80 is directed to a computer-readable medium containing substantially the same subject matter as claim 76. Therefore, each of the arguments for independent claim 76 also applies to independent claim 80 with equal force. Each of claims 77-79 depend from and will stand or fall with claim 76. After a concise discussion of the cited art, each ground of rejection to be reviewed on appeal is presented with separate heading and sub-heading as required by 37 C.F.R. § 41.37(c)(l)(vii). To aid in review of the Final Office Action (dated 24

November 2009), portions of the Final Office Action have been copied into this Brief.

A. Summary of Giles

Giles is directed to "[a]n emulation system [that] emulates operation of a graphics processor in a target computer system that is executing a computer program ... At each frame end the emulation module evaluates the ability of the general purpose computer to generate video frames fully synchronized with the target computer system. When the evaluation is positive, the emulation module fully executes all the commands ... when the evaluation is negative, the emulation module executes a first subset of the commands." Giles at Abstract. Stated another way, Giles discloses "a system and method for adaptively skipping video frames when the emulation system determines that emulation time is less than the real time of the system." Giles at Col. 1 lns. 10-13.

B. Summary of Glanville

Glanville is directed to a system for improving performance during graphics processing that involves application-programmable vertex processing that includes a CPU and a graphics application specific integrated

circuit (ASIC). Software is included to direct the ASIC to perform the graphics processing. The software can divide graphics code into a first and second portion. The second portion of the graphics processing includes application-programmable vertex processing unavailable by the graphics ASIC. The first portion of the graphics processing is executed on the ASIC and the second portion is executed on the CPU (because the ASIC has limitations or deficiencies). See Glanville at Abstract, ¶¶ 83-84. In summary, Glanville discloses modifying graphics code, if possible, to execute on an ASIC. If it is not possible to modify the code, Glanville discloses splitting the graphics code so that portions of the code that cannot be executed on the ASIC are executed on a CPU.

C. Claims 76-80 stand rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U.S. Patent No. 6,115,054 to Giles ("Giles") in view of U.S. Patent Publication No. 2003/0009748 to Glanville et al. ("Glanville")

Independent claims 76 and 80

The Examiner has rejected each of independent claims 76 and 80 as allegedly being obvious over Giles in view of Glanville. The Examiner has rejected independent claim 76 as follows:

> 8. Regarding claim 76, Giles teaches: A method of applying two effects to an image, the method comprising the steps of - using a first microprocessor to apply a first effect to a first frame of said image, said first microprocessor applying said first effect while emulating a second microprocessor (fig. 11A, 384 see also col. 16 lines 23-35) (The generation of frames is equivalent to applying a first effect).

Final Office Action dated 24 November 2009 at p. 4.

The Examiner asserts that "generation of frames is equivalent to applying a first effect." Final Office Action dated 24 November 2009 at p. 2. However, this is clearly incorrect because the plain language of the claim states "to apply a first effect ***to*** a first frame of said image." Because the effect is being applied to a frame, the frame must have already been generated. In the context of Giles the "generation of frames" has to do with a timing function

of the emulator relative to the target computer system. As stated above, Giles monitors the time taken by the emulator to generate frames to determine if the emulator must skip frames in order to stay in sync. Therefore, the generation of frames disclosed in Giles is in no way equivalent to applying effects to frames.

The Examiner admits:

> 9. Giles doesn't teach: -using said second microprocessor to apply a second effect to said first-effected frame, applying said first effect to a next frame by said first microprocessor approximately during the time that said second microprocessor is applying said second effect to said first-effected frame.

Final Office Action dated 24 November 2009 at p. 4.

The Examiner relies on Glanville to supply this missing limitation by asserting:

> 10. The analogous prior art Glanville teaches: -using said second microprocessor to apply a second effect to said first-effected frame, applying said first effect to a next frame by said first microprocessor approximately during the time that said second microprocessor is applying said second effect to said first-effected frame (fig. 6, 606 see also [0084]) (The portion of graphics processing performed on ASIC is equivalent to 2nd processor applying effect to first frame) for the benefit of providing a set of API features that facilitate combining application-programmable vertex processing with existing 3D applications originally authored to use conventional vertex processing, and providing for API features that reduce the effort required to augment an existing 3D application to use application-programmable vertex processing.

Final Office Action dated 24 November 2009 at p. 4.

As stated above, Glanville is simply directed to ***splitting up the graphics code*** between an ASIC and a CPU. The code is not split with any recognition of frames. Rather the code is split via software analysis such that the CPU performs the operations that cannot be performed by the ASIC. This is made clear when Glanville explains "[s]uch second portion of the graphics processing includes application–programmable vertex processing unavailable by the graphics ASIC" (Glanville at ¶ 15) and "[s]uch second portion of the graphics processing is adapted to overcome the deficiency [of the ASIC] by utilizing the CPU" (Glanville at ¶ 84). *See also,* Glanville at ¶¶ 81-82 (method for overcoming deficiencies in the system).

Independent claim 76 recites, *inter alia*, "applying said first effect to a next frame by said first microprocessor ***approximately during the time*** that said second microprocessor is applying said second effect to said first-effected frame." Glanville is completely silent as to at least two of these elements. Glanville does not disclose any kind of temporal division of work between two processors because Glanville only discloses splitting code based on capabilities of processors ***not timing related to frames***. Furthermore, Glanville is completely silent as to applying effects to frames by one processor and then another processor. For at least these reasons, claim 76 cannot be

rendered obvious by any combination of Giles and Glanville. Therefore, the Examiner has failed to present a legitimate *prima facie* case of obviousness as required by law and Patent Office procedure. Appellant respectfully requests the Board reverse this rejection.

In response to previous arguments the Examiner asserts:

> 3. Examiner respectfully disagrees: Giles does teach generation of frames is equivalent to applying effects to frames, (see col. 2 lines 53-60) (Upon detecting a frame end, the emulation module executes…so as to at least partially render a frame…evaluates the ability of the general purpose computer to generate video frames fully synchronized with the target computer system.)

Final Office Action dated 24 November 2009 at p. 2.

However, the Examiner's statement "generation of frames is equivalent to applying effects to frames" is unsupported and unreasonable. It appears the Examiner is asserting that because Giles discloses only partially rendering a frame (because his disclosed emulation system simply cannot keep up with program execution) the system of Giles discloses applying affects to frames. It would appear *per se* unreasonable to interpret skipping processing because a system cannot keep up to be equivalent in any way to applying effects to frames as recited in independent claim 76. Appellant notes the Examiner is allowed broad interpretation but that interpretation must be "reasonable." *See*

M.P.E.P § 2111. For at least these reasons, Giles does not disclose claim elements as the Examiner asserts.

In an additional response to previous arguments the Examiner asserts:

> 5. Examiner respectfully disagrees: The code in Glanville is split with recognition of frames, (see [0321]) (If the current vertex program is nonexistent or the "point" is culled, the current raster position and its associated data become...); Thus Glanville teaches splitting code with recognition of frames because the current raster position is tracked. Glanville does disclose temporal division of work between two processors, (see [0070]) (A program can be split into two (2) parts with the CPU 106 emulating some of the computations, and the ASIC 102 executing the remainder); Further see [0061], (A particular hardware implementation (i.e., ASIC 102) may have timing latencies where the result of an instruction will not immediately be available for use as input to a subsequent instruction); Thus Glanville teaches because Glanville is concerned with timing latencies and dividing work.

Final Office Action dated 24 November 2009 at p. 2.

Here, the Examiner incorrectly asserts that "[t]he code in Glanville is split with recognition of frames." Glanville only discloses splitting code with respect to ***capabilities*** of processors (*i.e.,* CPU and ASIC). *See* Glanville at ¶ 15. Also, even though Glanville discloses splitting code across processors and separately makes mention of a concern for timing latencies in no way does Glanville disclose the specific temporal division of work recited in independent claim 76. With respect to "timing latencies," Glanville clearly discloses "[i]n such case, the vertex program extension **104** can be used ***to***

reorder instructions so that another non-dependent instruction can be executed in such time slot, thus improving the throughput of the program." Glanville at ¶ 61 (emphasis added). Clearly Glanville is concerned with reordering instructions based on hardware capabilities and not with regard to frames.

Further, while relying on Glanville, the Examiner simply makes an unsubstantiated conclusion that "[t]he portion of graphics processing performed on the ASIC is equivalent to 2nd processor applying effect to first frame." Final Office Action dated 24 November 2009 at p. 4. The Board is reminded that rejections based on obviousness cannot be sustained by mere conclusory statements. *See* M.P.E.P. 2143. Even if one were to accept the Examiner's unsubstantiated conclusion, Glanville simply does not disclose that the ASIC (Examiner's cited 2nd processor) is applying said second effect to said first effected frame ***approximately during the time*** that said first effect is being applied to a next frame by said first microprocessor as recited in independent claim 76. For at least these reasons, Glanville does not disclose claim elements as the Examiner asserts.

Because Giles does not teach that which the Examiner asserts, even if one were to accept the Examiner's interpretation of Glanville, the Examiner's

proposed combination would not render claim 76 obvious. Similarly, because Glanville does not teach that which the Examiner asserts, even if one were to accept the Examiner's interpretation of Giles, the Examiner's proposed combination would not render claim 76 obvious. In the instant case, Appellant submits that neither Glanville nor Giles teach that which the Examiner alleges and thus the combination of Giles and Glanville cannot render the claimed subject matter obvious.

Because Giles or Glanville, either alone or in combination, do not disclose each and every element in each rejected independent claim, the Examiner has failed to make a legitimate *prima facie* case of obviousness under 35 U.S.C. 103 or established Patent Office examining guidelines. Appellant respectfully requests the Board reverse this rejection.

Each of claims 77-79 depend from independent claim 76 discussed above. Because each independent claim is clearly patentable over the cited art as discussed above, so too are claims 77-79. Appellant respectfully requests the Board reverse this rejection.

D. Conclusion

For at least the reasons stated above, Appellants respectfully submit that all outstanding rejections should be reversed. Additionally, to the extent specific claims have not been addressed, these claims depend from one or more claims that are specifically addressed, and are therefore patentable for at least the same reasons as the claims specifically addressed. Appellants further believe that they have complied with each requirement for an appeal brief.

In the course of the foregoing discussions, Appellants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that other limitations may be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the cited prior art which have yet to be raised, but which may be raised in the future.

If any fees are required or have been overpaid, please appropriately charge or credit those fees to Deposit Account Number 501922/119-0036US.

Respectfully submitted,

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VIII. Claims Appendix

1 – 75. (Cancelled).

76. (Original) A method of applying two effects to an image, the method comprising the steps of

- using a first microprocessor to apply a first effect to a first frame of said image, said first microprocessor applying said first effect while emulating a second microprocessor;
- using said second microprocessor to apply a second effect to said first-effected frame, applying said first effect to a next frame by said first microprocessor approximately during the time that said second microprocessor is applying said second effect to said first-effected frame.

77. (Original) The method of claim 76 wherein the first microprocessor is a CPU and the second microprocessor is a GPU.

78. (Original) The method of claim 76 where emulation is effected through a virtual machine.

79. (Original) The method of claim 76 wherein emulation is effected through translating a GPU program to a CPU program.

80. (Previously presented) A computer-readable medium having computer executable instructions for performing the method recited in claim 76.

IX. Evidence Appendix

None.

X. Related Proceedings Appendix

None.